Refine Search

Search Results -

Terms	Documents
L14 same path	2

Database:

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JPO Abstracts Database
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IBM Technical Disclosure Bulletins

Search: L15

Refine Search

Recall Text Clear Interrupt

Search History

DATE: Wednesday, June 21, 2006 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L15	L14 same path	2	L15
L14	l5 same bypass	20	L14
L13	L12 same l4	27	L13
L12	embedded adj1 core	1834	L12
L11	L10 same unit	4	L11
L10	l5 same core	61	L10
	DB=USPT,PGPB; PLUR=YES; OP=OR		
L9	('4750155'| '4870302'| '4930098'| 'RE34363'| '5237219'| '5432719'| '5453706'| '6046603'| '6057704'| '6091263'| '6128215'| '6181158'| '6255849'| '6269020'| '6314539'| '6353551'| '6499124'| '6608500')![pn]	18	L9
	DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L8	L6 and l5	6	L8
L7	L6 same l5	0	L7

L6	L1 same l2	5664	L6
L5	L4 same configur$	569	L5
L4	scan adj1 chain	2464	L4
L3	L2 same l1	5664	L3
L2	second adj1 configuration	11815	L2
L1	first adj1 configuration	12405	L1

END OF SEARCH HISTORY

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

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L8: Entry 2 of 6 File: USPT Jan 11, 2005

DOCUMENT-IDENTIFIER: US 6842039 B1
TITLE: Configuration shift register

Brief Summary Text (16):
The present invention provides an electronic device having configuration elements connected as a shift register, the configuration elements being relevant to a particular programmable function or subset of programmable functions such as I/O. The configuration shift register may be loaded with new data without having to reprogram other configuration elements of the electronic device. In an exemplary embodiment, the electronic device is a programmable logic device (PLD). In an aspect of an exemplary embodiment, shadow register elements allow programming data from one configuration to be maintained for particular IOs while new programming data for another configuration is loaded into the configuration shift register. In an aspect of a particular embodiment, a JTAG port of the PLD is used to load data into the configuration shift register and a demultiplexer selectively directs data to either a boundary scan chain of elements used for JTAG test data or to the configuration shift register. In another aspect of a particular embodiment, selected configuration elements in the configuration shift register are connected to pins for parallel loading of configuration data as an alternative to sequential loading of data into the configuration shift register from a single pin. In an alternative embodiment, cells of configuration elements forming the configuration shift register are interleaved with cells of elements used for JTAG test data forming a single shift register that may be used for rapidly reconfiguring particular programmable functions of the electronic device and also may be for boundary scan test purposes.

Drawing Description Text (4):
FIG. 2 is another diagram of the programmable logic device of FIG. 1 highlighting implementation of the configuration shift register of FIG. 1 relative to a boundary scan chain for JTAG testing wherein an input pin utilized for JTAG test data may also be used for inputting data to the configuration shift register.

Drawing Description Text (7):
FIG. 5 shows an alternative implementation of a configuration shift register in a PLD relative to a boundary scan chain.

Detailed Description Text (13):
Demultiplexer ("demux") 240 and multiplexer ("mux") 260 allows configuration shift register 200 to share, respectively, an input pin and an output pin with boundary scan chain 300, as discussed in more detail in relation to FIG. 2.

Detailed Description Text (14):
FIG. 2 is a view of PLD 20 of FIG. 1 that highlights the implementation of configuration shift register 200 relative to a boundary scan chain ("BSC") 300 used for implementing the Joint Test Action Group ("JTAG") specification requirements. The JTAG specification requires dedicated elements, typically organized as a chain of cells each cell having elements for holding three bits per cell. This chain of dedicated elements is used to facilitate the testing of integrated circuit devices. Such a chain is referred to as "Boundary Scan Chain" or "BSC." BSC 300 is made up of BSC elements 301.

Detailed Description Text (26):
FIG. 5 shows an alternative implementation of configuration shift register cells relative to boundary scan chain cells. In the implementation shown in FIG. 5, alternating cells 520 and 530 are combined to form a shift register 500 in PLD 50 (i.e. cells 520 and 530 are interleaved). I/O configuration shift register cells 520 of flip flops 510 are coupled to corresponding I/O blocks 525 for providing I/O configuration bits driving I/O blocks 525 to one of multiple prescribe configuration states. Boundary scan elements 531 (grouped into cells 530) each may hold data bits relevant to JTAG boundary scan testing. During testing, proper loading of I/O configuration data into shift register 500 for repeated I/O testing can be ensured by accounting for the number of BSC cells 530 of BSC elements 531 between each of the I/O configuration cells 520 of I/O configuration flip flops 510.

CLAIMS:

1. An integrated circuit comprising: a plurality of I/O blocks; a plurality of I/O configuration elements including outputs, the I/O configuration elements being coupled together as a shift register on a periphery of the integrated circuit, and the I/O configuration elements also being coupled to the plurality of I/O blocks for driving, each of the plurality of I/O blocks to one of multiple prescribed I/O configuration states based upon configuration bits provided at the outputs of the plurality of I/O configuration elements; a boundary scan chain comprising a plurality of boundary scan elements; a first pin; and a demultiplexer including at least an input, a first output, and a second output, the input being coupled to the first pin, the first output being coupled to a first one of the plurality of I/O configuration elements, the second output bin coupled to the boundary scan chain, the demultiplexer being for selecting either the configuration shift register the bound scan chain to receive data through first pin.

5. An integrated circuit comprising: a plurality of I/O blocks; and a multiple input shift register including: a plurality of configuration elements coupled to the shift data between configuration elements; and a plurality of respective multiplexers respectively coupled between respective pairs of configuration elements, the respective multiplexers respectively including a respective first multiplexer input coupled to a data source external to the sift register, a respective second multiplexer input connected to a respective first configuration element of a respective pair of configuration elements, and a respective multiplexer output connected to a respective second configuration element of the respective pair of configuration elements; wherein configuration elements of the shift register are coupled to drive respective I/O blocks to prescribed configuration states.

18. A method of configuring I/O blocks of an electronic device comprising: providing I/O configuration elements coupled together as a shift register on a periphery of the electronic device and coupled for driving the I/O blocks to one of a plurality of prescribed states; loading configuration data into the I/O configuration elements; providing a demultiplexer including an input coupled to an input pin of the electronic device, a first output coupled to a boundary scan chain and a second output coupled to at last one of the plurality of I/O configuration elements; when loading boundary scan chain test data through the input pin, causing the demultiplexer to select the first output coupled to the boundary scan chain; and when loading I/O configuration data through the input pin, causing the demultiplexer to select the second output coupled to the at least one of the plurality of I/O configuration elements.

24. An integrated circuit including circuitry controlled by programmable elements, the integrated circuit comprising: first programmable elements coupled together to form a shift register; second programmable element coupled to at least some of the

first programmable element so that second configuration data can be shifted into the first programmable elements without displacing first configuration data previously stored in the second programmable elements; a first clock signal line coupled to the first programmable element; and a second clock signal line coupled to the second programmable elements; wherein the first programmable elements shift data in response to a signal on the first clock signal line and the second programmable elements latch data from at least some of the first programmable elements in response to a signal on the second clock signal line.

25. An integrated circuit including circuitry controlled by programmable elements, the integrated circuit comprising: first programmable elements coupled together to form a shift register; second programmable elements coupled to at least some of the first programmable elements so that second configuration data can be shifted into the first programmable elements without displacing first configuration data previously stored in the second programmable elements; and multiplexers coupled to receive as inputs data provided by first and second programmable elements and coupled to provide as a selected output either data provided by the first programmable elements or data provided by the second programmable elements wherein the selected output is provided to circuitry controlled by the either of the first and second programmable elements.

26. A method of configuring and reconfiguring circuitry of an electronic device comprising: providing first configuration elements coupled together as a shift register and coupled to circuitry controlled by the first programmable elements; providing second configuration elements coupled to circuitry controlled by the second configuration elements and coupled to at least some of the first configuration elements; loading first configuration data into the first configuration elements; latching at least some of the first configuration data from at least some of the first configuration elements into the second configuration elements; and loading second configuration data into the first configuration elements.

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
End of Result Set

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L11: Entry 4 of 4 File: USPT Aug 1, 2000

DOCUMENT-IDENTIFIER: US 6097988 A
TITLE: Logic system and method employing multiple configurable logic blocks and capable of implementing a state machine using a minimum amount of configurable logic

Detailed Description Text (26):
FIG. 5 is a block diagram of a preferred embodiment of each CLB 12. CLB 12 is configured to facilitate Joint Test Action Group (JTAG) boundary-scan testing of internal circuitry according to IEEE Standard 1149.1-1990. Constructs of the testing architecture are also used to configure the programmable logic within CLB 12 to perform the one or more functions required in any state of the state machine. CLB 12 includes multiple boundary scan cells 44 inserted between corresponding I/O signal lines 46 and a core logic 48. Boundary scan cells 44 are controlled by a CLB control unit 50. When the enable signal from control unit 16 is asserted, signals upon I/O lines 46 flow to and from core logic 48 unimpeded. When the enable signal is deasserted, signals upon I/O lines 46 are disconnected from core logic 48 by placing boundary scan cells 44 in a high impedance state. In a testing mode and a programming mode, CLB control unit 50 configures boundary scan cells 44 to form a serial "scan chain" surrounding core logic 48. Input values, produced by control unit 16, are shifted through the scan chain, then applied to the core logic. In the testing mode, output values produced by core logic 48 are captured by a number of the boundary scan cells 44 and shifted out through the scan chain. Control unit 16 compares the output values to expected values. In the programming mode, the input signals applied to core logic 48 are used to configure programmable switching elements within core logic 48. As a result, core logic 48 is caused to implement the one or more logic functions of a state.

Previous Doc Next Doc Go to Doc#

L15: Entry 2 of 2 File: USPT Sep 2, 2003

DOCUMENT-IDENTIFIER: US 6615380 B1
TITLE: Dynamic scan chains and test pattern generation methodologies therefor

Detailed Description Text (19):
Specifically, in the illustrated embodiment, the output 431 of cell 420a is coupled to a first input of bypass mux 490a. The SI input of the cell 420a is coupled to other scannable memory cells or a primary input if cell 420a is the first cell of the scan chain 400. Additionally, the SI input of the cell 420a is coupled to a second input of the bypass mux 490a. The output of the bypass mux 490a is routed to mission mode circuitry 405a of the combinational logic 405 and is also routed to another scannable memory cell 420b or to a primary output, if this cell 420a-is the last cell of a scan chain 400. When the first input of the bypass mux 490a is selected, the scan cell 420a will be included in the scan path. When the second input of the bypass mux 490a is selected, the scan cell 420a will be excluded (or "bypassed") in the scan path. Bypass muxes 490a-490e are controlled by configuration signals BYPASS_0, BYPASS_1, BYPASS_2, BYPASS_3, and BYPASS_4, respectively.

Detailed Description Text (21):
According to the present embodiment, during mission mode (e.g., when SE lines are not asserted), the configuration signals are not asserted such that normal operations of the integrated circuit design can be carried out. During test mode (e.g., when SE lines are asserted), each scan cell 420a-420e could be included or bypassed with the appropriate assertion of the configuration signals. For example, scan cell 420a could be bypassed when BYPASS_0 is asserted, and scan cell 420d could be bypassed when BYPASS_3 is asserted. FIG. 2B illustrates several exemplary test patterns T10-T15 applicable to scan chain 400 of the present embodiment. As illustrated in FIG. 2B, exemplary test patterns T10-T15 require only some of the scan cells 420a-420e to be included in the scan path. For instance, test pattern T10 requires only scan cell 420a, 420b and 420e; and test pattern T14 requires only scan cell 420c, 420d and 420e to be included. The unspecified inputs are marked with and the corresponding scan cells are bypassed by the assertion of the appropriate configuration signals. For example, when test pattern T10 is applied, configuration signals BYPASS_2 and BYPASS_3 are asserted to bypass scan cells 420c and 420d. The resultant dynamically constructed scan chain is then made of scan cells 420a, 420b and 420e.

Detailed Description Text (25):
In operation, scan chain 500 can be dynamically reconfigured into one of three different scan configurations: a full scan with both segments 510a and 510b included as a single chain, a partial scan with segment 510a only or another partial scan with segment 510b only. More specifically, in the present embodiment, segments 510a and 510b are included in the scan path when BYPASS_A and BYPASS_B are not asserted. Segment 510a is excluded when BYPASS_A is asserted and segment 510b is excluded when BYPASS_B is asserted. Routing congestion is released in this case because reconfiguration logic of scan chain 500 includes only two bypass muxes 530a and 530b.